R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found, for example, in claims 1 and 2, as originally filed. Thus, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 3, 13 and 15 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §101

The rejection of claim 13 under 35 U.S.C. §101 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 13 and 20 under 35 U.S.C. §102(b) as being anticipated by Ohuchi '847 is respectfully traversed and should be withdrawn.

Ohuchi concerns a data processor with wait control allowing high speed access (Title).

Claim 1 provides (in part) a bus comprising a master interface configured to receive an early command signal having a predetermined timing relationship to a first clock edge. Despite the assertion in the Office Action, FIG. 5 of Ohuchi does not appear to disclose a predetermined timing relationship between a signal WRRQ (asserted similar to the claimed early command signal) and an edge of a signal CLK (asserted to define the claimed first clock edge). Therefore, *prima facie* anticipation has not been established.

Claim 1 further provides a slave interface configured to present a command signal a delay after the first clock edge. Despite the assertion in the Office Action, a signal WRRQIO (asserted similar to the claimed command signal) does not appear to be presented at a slave interface of a system bus 20 as presently claimed. In particular, Ohuchi states that the signal WRRQIO, is an internal signal within a slave processor 12 (see column 3, lines 47-50 of Ohuchi). The rejection appears to be arguing a structure different than as claimed. As such, Ohuchi does not disclose or suggest a slave interface configured to present a command signal as presently claimed.

Furthermore, Ohuchi appears to be silent and the Office Action provides no evidence that the signal WRRQIO of Ohuchi is presented a delay after the first clock edge as presently claimed. In contrast, FIG. 4 of Ohuchi appears to suggest that the signal

WRRQIO is set independently of the signal CLK. Therefore, *prima facie* anticipation has not been established.

Claim 1 further provides the slave interface configured to receive a slave wait signal. Despite the assertion in the Office Action, the signal WAITI does not appear to be presented at a slave interface of the system bus 20 of Ohuchi. In particular, Ohuchi shows that the signal WAITI is an internal signal within the slave processor 12 (see FIG. 4 of Ohuchi). The rejection appears to be arguing a structure different than as claimed. As such, Ohuchi does not disclose or suggest a slave interface configured to receive a slave wait signal as presently claimed.

Claim 1 further provides the bus comprising a control logic configured to register the early command signal to generate the command signal. Despite the assertion in the Office Action, FIGS. 2 and 3 and the text in column 3, lines 35-53 of Ohuchi do not appear to discuss a circuit of the system bus 20. In contrast, the cited sections of Ohuchi appear to discuss circuitry within the slave processor 12. Therefore, Ohuchi does not disclose or suggest a bus comprising a control logic configured to register an early command signal to generate a command signal as presently claimed.

Claim 1 further provides the control logic configured to convert the slave wait signal into a bus wait signal (presented at a master interface of the bus). Despite the assertion in the Office Action, FIGS. 2 and 3 and the text in column 3, lines 56-61

of Ohuchi appear to be silent regarding (i) a circuit of the system bus 20 converting the signal WAITI into the signal WAIT (asserted similar to the claimed bus wait signal) and (ii) presenting the signal WAIT at a master interface of the system bus 20. Therefore, Ohuchi does not disclose or suggest a control logic configured to convert a slave wait signal into a bus wait signal (presented at a master interface) as presently claimed. Claims 13 and 20 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 8, 9 and 14 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in view of Amagasaki '080 is respectfully traversed and should be withdrawn.

The rejection of claims 3 and 15 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Amagasaki in further view of Honma '662 is respectfully traversed and should be withdrawn.

The rejection of claims 4 and 16 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in view of McIntyre '261 is respectfully traversed and should be withdrawn.

The rejection of claims 5, 6, 17 and 18 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi in further view of U.S. Patent Application Publication No. 2001/0010063 to Hirose et al.

(hereafter Hirose) is respectfully traversed and should be withdrawn.

The rejection of claims 7 and 19 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Hirose in further view of Pincus '583 is respectfully traversed and should be withdrawn.

The rejection of claims 10, 11 and 12 under 35 U.S.C. §103(a) as being unpatentable over Ohuchi and Amagasaki in further view of Picazo '907 is respectfully traversed and should be withdrawn.

Ohuchi concerns a data processor with wait control allowing high speed access (Title). Amagasaki concerns an integrated circuit device having tristate input buffer for reducing internal power use (Title). Hirose concerns a bus controller system for integrated circuit device with improved bus access efficiency (Title). Honma concerns a memory testing device for preventing excessive write and erasure (Title). McIntyre concerns a method and apparatus for burst protocol in a data processing system (Title). Picazo concerns a network hub with integrated bridge (Title). Pincus concerns a method and apparatus for memory access in a matrix processor computer (Title).

The Office Action fails to establish that Honma and Pincus are analogous art. The main reference Ohuchi has a primary U.S. classification of 364/200. Honma has a primary U.S. classification of 371/21.1. Pincus has a primary U.S.

classification of 709/400. As such, the U.S. classification system suggests that Honma and Pincus are non-analogous art relative to Ohuchi.

Furthermore, no evidence has been provided in the Office Action that Honma and Pincus are either (i) within the Applicant's field of endeavor or (ii) reasonably pertinent to the particular problem with which the Applicant was concerned (MPEP §2141.01(a)). Due to a lack of evidence to the contrary, the U.S. Patent and Trademark Office classifications appear to show that Honma and Pincus are non-analogous art and thus the proposed combinations are not obvious. As such, claims 3, 7, 15 and 19 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 provides the master interface is configured to receive an early address signal having the predetermined timing relationship with the first clock edge. Despite the assertion in the Office Action, FIG. 2 of Ohuchi does not appear to show any relationship between a signal ADDRESS (asserted similar to the claimed early address signal) and the signal CLK (asserted to define the claimed first clock edge). Therefore, *prima facie* obviousness has not been established.

Claim 2 further provides the address signal is presented by the slave interface the delay after the first clock edge. Despite the assertion in the Office Action, FIG. 5 of Ohuchi does not appear to show a signal AREG (asserted similar to the claimed

address signal) either (i) being presented at a slave interface of the system bus 20 nor (ii) having a delay after a first clock edge of the signal CLK. Therefore, *prima facie* anticipation has not been established. Claim 14 provides language similar to claim 2. As such, claims 2 and 14 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 9 provides the control logic comprises a plurality of registers configured to register a plurality of early signals each having the predetermined timing relationship with the first clock edge. Despite the assertion in the Office Action, elements 42 and 44 in FIG. 3 of Ohuchi appear to be silent regarding a predetermined timing relationship between any signals and the signal CLK. Therefore, Ohuchi and Amagasaki, alone or in combination, do not teach of suggest a control logic comprising a plurality of registers configured to register a plurality of early signals each having a predetermined timing relationship with a first clock edge as presently claimed. As such, claim 9 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 3 provides the master interface is configured to receive a no-address signal having the predetermined timing relationship with the first clock edge. Despite the assertion in the Office Action, element 3A in FIG. 5 and the text in column 6, lines 35-41 of Honma appear to be silent regarding a signal S1

(asserted similar to the claimed no-address signal) having a predetermined timing relationship with a clock edge. Therefore, Ohuchi, Amagasaki and Honma, alone or in combination, do not teach or suggest a master interface configured to receive a no-address signal having a predetermined timing relationship with a first clock edge as presently claimed. Claim 15 provides language similar to claim 3. As such, claims 3 and 15 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 4 provides the master interface configured to receive an early burst request signal having the predetermined timing relationship with the first clock edge. In contrast, the Office Action fails to present evidence that Ohuchi and/or McIntyre teach or suggest an early burst request signal having a predetermined timing relationship with a first clock edge as presently claimed. Therefore, *prima facie* obviousness has not been established.

Claim 4 further provides a burst request signal presented a delay after the first clock signal from the slave interface. In contrast, the Office Action fails to present evidence that Ohuchi and/or McIntyre teach or suggest a burst request signal presented a delay after a first clock signal from a slave interface as presently claimed. Therefore, *prima facie* obviousness has not been established. Claim 16 provides language similar to claim 4. As

such, claims 4 and 16 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 5 provides the master interface is configured to (i) receive a bus request signal and (ii) present a bus grant signal. Despite the assertion in the Office Action, page 4 paragraph 67 of Hirose appears to be silent regarding request and grant signals being received and presented at a master interface to a bus 100. The rejection appears to be arguing a structure different than as claimed. Therefore, *prima facie* obviousness has not been established. Claim 17 provides language similar to claim 5. As such, claims 5 and 17 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 6 provides the control logic is configured to present the command signal (at the slave interface per claim 1). Despite the assertion in the Office Action, FIG. 5B and the text on page 4, paragraph 65 of Hirose appears to be silent regarding a command signal B1 (asserted similar to the claimed command signal) being presented at a slave interface as presently claimed. Therefore, Ohuchi and Hirose, alone or in combination, do not teach or suggest a control logic configured to present a command signal (at a slave interface) as presently claimed. Claim 18 provides language similar to claim 6. As such, claims 6 and 18 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 7 provides the master interface is configured to receive a lock signal. Despite the assertion in the Office Action, FIG. 13A and the text in column 24, lines 9-19 of Pincus appears to be silent regarding a master interface receiving a lock signal as presently claimed. Therefore, *prima facie* obviousness has not been established. Claim 19 provides language similar to claim 7. As such, claims 7 and 19 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 12 provides a first multiplexer (from claim 11) and a second multiplexer configured to select a write data select signal responsive to a bus grant signal. In contrast, each of Ohuchi, Amagasaki and Picazo appear to be silent regarding a second multiplexer selecting a write data select signal as presently claimed. Furthermore, of the three elements 610, 640 and 650 (in FIG. 6B of Picazo) cited by the Office Action, only element 610 appears to be a multiplexer. However, the element 610 is already asserted in the Office Action to be similar to the claimed first multiplexer. Therefore, Ohuchi, Amagasaki and Picazo, alone or in combination, do not teach or suggest a first multiplexer and a second multiplexer configured to select a write data select signal responsive to a bus grant signal as presently claimed. As such, claim 12 is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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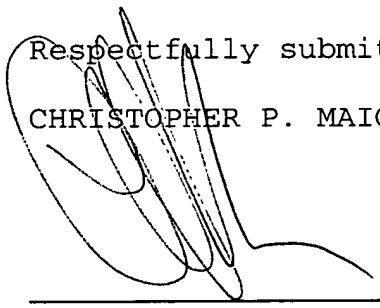

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